SHORT-FORM DATA

CCD42-20-*-D21 \FT version

2048 x 1024 Pixel Back-illuminated Deep-depletion Scientific CCD Sensor

Features

- 2048 x 1024 pixel image area
- Back Illuminated Operation
- Deep depletion silicon for enhanced red response
- 13.5 µm Square Pixels
- Low Noise, high responsivity
- output amplifiers
- 42pin ceramic/metal Package
- Gated dump drain on output register
- Symmetrical anti-static gate protection

Introduction

This version of the CCD42 family of CCD Sensors has full frame architecture. Back illumination technology in combination with an extremely low noise amplifier make the device well suited to the most demanding applications such as astronomy.

The output amplifier is designed to give excellent noise levels at low pixel rates and can match the noise performance of most conventional science CCDs at pixel rates as high as 1 MHz.

The readout register has a gate controlled dump drain to allow fast dumping of unwanted data. The register is designed to accommodate 4 image pixels of charge and a summing well is provided capable of holding 6 image pixels. The output amplifier has a feature to enable the responsivity to be reduced to allow the reading of such large charge packets.

The device is supplied in a 42 pin ceramic package designed for ease of use. The design of the package permits easy housing to cold shoes or supports.

The CCD42-20 is also available in front illuminated format or on a metal package designed for close butting.

General Data

Format

Image Area	(mm)	27.6 x 13.8
Active Pixels	(H)	2048
	(V)	1024 + 4
Pixel Size	(µm)	13.5 x 13.5
Number of output amplifiers		2
Number of underscan pixels		50
100% fill factor		

Package

Format	Ceramic/metal with 42 pin connections
Size	48 x 37mm

Performance (typical also shown)

Min. O/P Amp Responsivity	(µV/e-)	3	(4.5)
Min. Peak Signal	(ke-/pixel)	100	(150k)
Min. Register charge capacity	(ke)	200	(400)
Min. Summing well charge capacity	(ke)	400	(600)
Min. Charge Transfer Efficiency	(%)		
Parallel	99.999	(99.9998)	
Serial	99.999	(99.9995)	
Min. Quantum Efficiency	400nm	25%	(40)
	500nm	60%	(70)
	650nm	85%	(95)
	900nm	45%	(55)
Minimum Spectral Range	(nm)	200 - 1100	
Max. Readout Noise (140-230K)	(e- rms)	4	(3)
Max. Dark current at –120C	(e^-/pix/hr)	4	(0.01)
Dark signal at 20C	(e-/pix/sec)	20,000	

Note: All values quoted using typical operating conditions at a readout frequency of 20 kHz and at a temperature of 173K (approx).

The device has the ER1 (enhanced red) coating for optimized red wavelength use.

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Typical Operating Conditions

Ref:	Pin No.	Description	Typ.Voltage
Vss	1,13,28,40	Substrate	9V
Iϕ1	6,39	Store Image clock	12V
Iϕ2	7,34	Store Image clock	12V
Iϕ3	5,38	Store Image clock	12V
FT1	3,42	FT image clock	12V
FT2	2,41	FT image clock	12V
FT3	4,37	FT image clock	12V
Rϕ1(L)	20	Register clock	11V (note 1)
Rϕ2(L)	19	Register clock	11V (note 1)
Rϕ1(R)	23	Register clock	11V (note 1)
Rϕ2(R)	22	Register clock	11V (note 1)
Rϕ3	24	Register clock	11V
ϕR(L)	18	Reset clock	12V
ϕR(R)	27	Reset clock	12V
ϕSW(L)	20	Summing Well	11V
ϕSW(R)	25	Summing Well	11V
DG	26,17	Register Dump Gate	0V (note 2)
OG1(L)	15	Output gate-1	3V
OG1(R)	30	Output gate-1	3V
DD	32,11	Dump drain	24V
OG2(L)	14	Output gate-2	See Note 3
OG2(R)	29	Output gate-2	See Note 3
OD(L)	10	Output drain	29V
OD(R)	31	Output drain	29V
OS(L)	9	Output source	See Note 4
OS(R)	36	Output source	See Note 4
RD(R)	33	Reset drain	17V
RD(L)	12	Reset drain	17V
NC	21		

General Note

Readout register clock pulse low levels +1V.
Other clock low levels 0 ± 0.5V.

Note 1

With the Rϕ connections shown this device will operate through both outputs. In order to operate from the left hand output only Rϕ1 and Rϕ2 should be reversed.

Note 2

Non charge-dumping level shown.
For charge dumping DG should be pulsed to 12 +/- 2V

Note 3

OG2 = OG1 + 1 volt - normal low noise Mode.

or = 20v - Low responsivity / increased charge Handling mode.

Note 4

OS = 3 - 5 volts below OD typically.

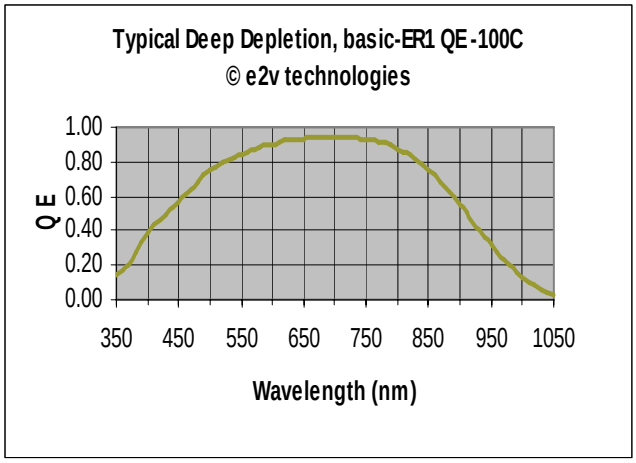
Blemish Specification

Grade	0	1	2
Column Defects	0	2	6
Black Defects	50	75	150
Traps > 200e-	2	5	12
White Defects	60	80	120

Maximum number of defects is shown.

Grade-5 devices are also available for setup purposes, but have no associated blemish specification; other performance levels are also not guaranteed.

Quantum Efficiency



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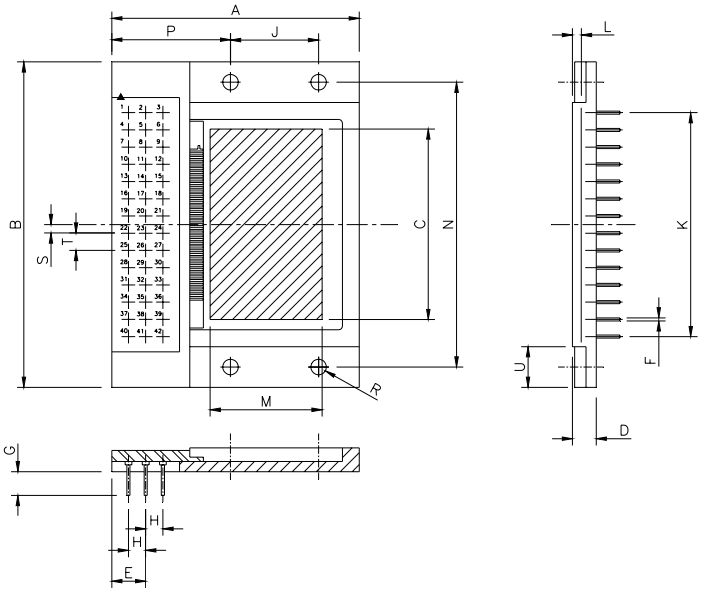

PIN CONNECTIONS

1	SS	2	(FT2)	3	(FT1)
4	(FT3)	5	IØ3	6	IØ1
7	IØ2	8	LS	9	OSL
10	ODL	11	DD	12	RDL
13	SS	14	OG2L	15	OG1L
16	ØSWL	17	DG	18	ØRL
19	RØ2L	20	RØ1L	21	–
22	RØ2R	23	RØ1R	24	RØ3
25	ØSWR	26	DG	27	ØRR
28	SS	29	OG2R	30	OG1R
31	ODR	32	DD	33	RDR
34	IØ2	35	LS	36	OSR
37	(FT3)	38	IØ3	39	IØ1
40	SS	41	(FT2)	42	(FT1)

REF	MILLIMETERS
A	36.50 ±0.20
B	48.00 ±0.20
C	28.10 ±0.20
D	3.50 ±0.20
E	5.00 ±0.38
F	ø0.45 ±0.10
G	3.50 ±0.20
H	2.54 ±0.13
J	13.00 ±0.20
K	33.02 ±0.20
L	1.30 ±0.20
M	16.50 ±0.20
N	42.00 ±0.20
P	17.50 ±0.20
R	ø2.30 ±0.20
S	1.27 ±0.13
T	2.54 ±0.13
U	6.00 ±0.20